

## Master thesis

# Implementation and evaluation of an FPGA accelerated image-processing module for edge computing platforms

## Topic and goal of the thesis

With the advancing automation of vehicles, edge computing tasks become an increasingly important research topic. These tasks require powerful hardware, which at the same time consumes as little energy as possible. FPGAs are a particularly well suited solution for such cases.

One of those cases are Intelligent Transport Systems Stations (ITS-S). These stations are used in the research and development of automated vehicles and record a large amount of data in the form of camera videos and LiDAR point clouds. The processing of this data requires state-of-the-art computer vision algorithms and neural networks, which are computationally expensive. A particular challenge is to maintain the real-time capability of such algorithms. The goal of this thesis is to implement and integrate an existing software pipeline to a high-end FPGA module, which is able to process the recorded data under the aspects of energy efficiency and real-time capability.

This thesis will be supervised in cooperation with the Chair of Integrated Digital Systems and Circuit Design (IDS). The contact on part of the IDS will be Cecilia Latotzke, M.Sc. ([latotzke@ids.rwth-aachen.de](mailto:latotzke@ids.rwth-aachen.de)).

## Tasks

- Literature research on suitable methods to implement the task
- Implementation of an existing software pipeline to an FPGA module using the chosen method
- Evaluation of the implementation regarding power usage, processing time, maximum complexity of the pipeline, ...

## Your profile

- Good English and German language skills
- Reliability, commitment and enjoyment of working independently
- FPGA programming experience
- Basic machine learning experience

## Department

Vehicle Intelligence & Automated Driving

## Contact



Amarin Klöcker, M.Sc.

☎ +49 241 80 25589

✉ [amarin.kloeker@ika.rwth-aachen.de](mailto:amarin.kloeker@ika.rwth-aachen.de)

## Language

German and English

## Entry Date

Earliest possible date

## Prior knowledge

FPGA Programming knowledge

Basic machine learning experience